REMARKS

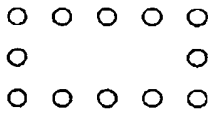
Claims 1, 2, and 5 are presently active.

In the Office Action dated 16 July 2003 ("Office Action"), claims 1, 2, and 5 were rejected under 35 U.S.C. §102(e) as being anticipated by Harada, et al., US patent 6,198,362 ("Harada").

Applicants do not believe that Harada is applicable to the present invention. The Office Action makes reference to Figs. 1 and 2 of Harada, and identifies (8) with a first agent; leftmost (7) with the first array of vias; rightmost (7) with the second array of vias; and (6) with the bus traces. (I'll assume that the rightmost (8) would have been identified in the Office Action with the second agent.)

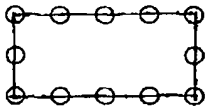
Upon reading Harada, column 6, it is seen that (6) is a top layer power supply pattern. (See column 6, line 26.) The shape of (6) is a belt-shaped conductive pattern such as a conductive loop on the periphery of a printed circuit board. (See column 6, line 20.) Note that (3) in Fig. 2 is a power supply layer, and that leftmost vias (7) connect the leftmost top layer power supply pattern (6) to power supply layer (3), and that the rightmost vias (7) connect the rightmost top layer power supply pattern (6) to power supply layer (3).

Applicants do not see a set of channels defined by the vias. Supposedly, although not explicitly shown, vias 7 would be connected to a top layer power supply pattern at regular intervals. Because the top layer power supply pattern is "belt-shaped", vias 7 would form a rectangular pattern, such as shown below in simplified form when looking downward into the printed circuit board.



It is not clear where the set of channels is as required by the claims. As described in the specification of the present application, page 4, line 10, "The region between two consecutive rows (or columns) of a regular array of vias define a channel." Referring to the above diagram in this Office Response, would the channel be between the two rows

and columns of the above rectangle? If so, then there is no bus that is routed in this "channel", as required by the claims, because top layer power supply pattern (6) would be above the vias to also form a "belt-shape" conductive path. (See the simplified diagram below.) It wouldn't lie "between two consecutive rows or columns of a regular array of vias."



Furthermore, the claims require that "each bus trace is routed in only one channel belonging to the first set of channels and routed in only one channel belonging to the second set of channels." Even if top layer power supply pattern (6) were to somehow be identified as routed in one channel belonging to the first set of channels, it certainly is not routed to the other agent so as to also be routed in only one channel belonging to the second set of channels.

Accordingly, Applicants do not believe that the presently active claims are taught or suggested by Harada.

Respectfully submitted,

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